JRO digital receiver modernization using ADCs with high-speed JESD204B data interface and FPGAs

J. Verastegui[1], J. Rojas[1], I. Tupac[1] , D. Caceres[1], L. Gonzales[1]

[1]Radio Observatorio de Jicamarca, Instituto Geosfísico del Perú, Lima, Perú

Abstract

The latest data acquisition system running at the Jicamarca Radio Observatory for the main radar has been used for more than five years now. Although there are no major inconveniences on the performance there have been some problems with internal interferences which are usually unpredictable and related to the PCB design, the noise floor can be different between channels too. So there are some chances of improvement developing a new approach. We propose a new design based on a high-speed JESD204B data interface; the digital signal processing and custom acquisition logic will be implemented inside an FPGA capable of managing the JESD204B high-speed interface. This will give us the flexibility of implementing digital blocks inside the FPGA to improve the performance of the receivers, we will gain scalability to perform on a much higher bandwidth and the PCB will be very much simplified which will reduce the manufacturing costs, design time, and development time.

1. Introduction

The JARS 2.0 system, our latest acquisition system, is composed of three main boards, the bus board, which transfer and packs the data, the control board, which configure and transmits all the data to the PC and the receiver board. We have thought in a way to not totally replace every part of the system, we have focused on the most critical part, which is the receiver boards. The receiver board, showed on Figure 1, is mainly based on two integrated circuits the AD6645 which is a 14 bit ADC and the AD6620 which is a digital receiver circuit. In summary the receiver does all the DSP operations needed for the processing of the radar data. All the traces are connected as single ended signals and there are also some sticky logic gates for control, which causes some synchronization problems.

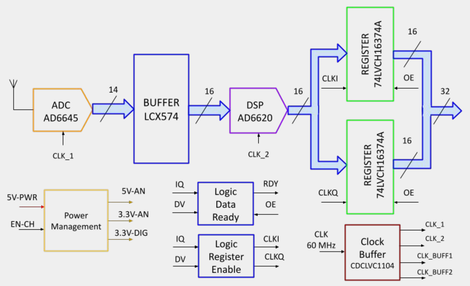
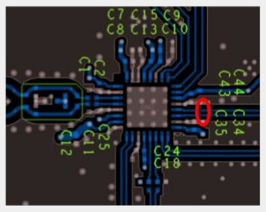


Figure 1. JARS 2.0 Receiver block diagram

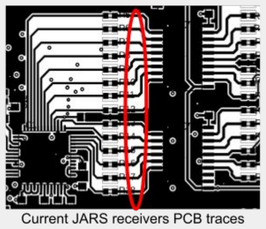
2. JESD204B High Speed Interface

We will use a high speed interface for the acquired data, we propose to design a JESD204B based architecture for our digital receivers. The JESD204B is a very versatile and very fast protocol to be used for data converter systems. Figure 2 shows the different benefits on using
the JESD204B protocol. We only need to guarantee the use of GTX drivers on the Kintex 7 FPGA from Xilinx.

1. Reduce crosstalk and improve synchronization between signals
2. Reduce complexity and area of PCB designs
3. Less power consumption in comparison to LVDS
4. Very high speed data bandwidth
5. Standardized protocol designed by a group of very reliable companies



JESD204B (ADC14X250) PCB traces



Current JARS receivers PCB traces

Figure 2. JESD204B Protocol Benefits

3. PCB block diagram

Figure 3 shows the PCB block diagram of our proposed design. The FPGA will not only handle the JESD204B but also will manage the DSP operations needed. The AD9250 is a dual channel ADC so we'll only need one IC for each receiver board.

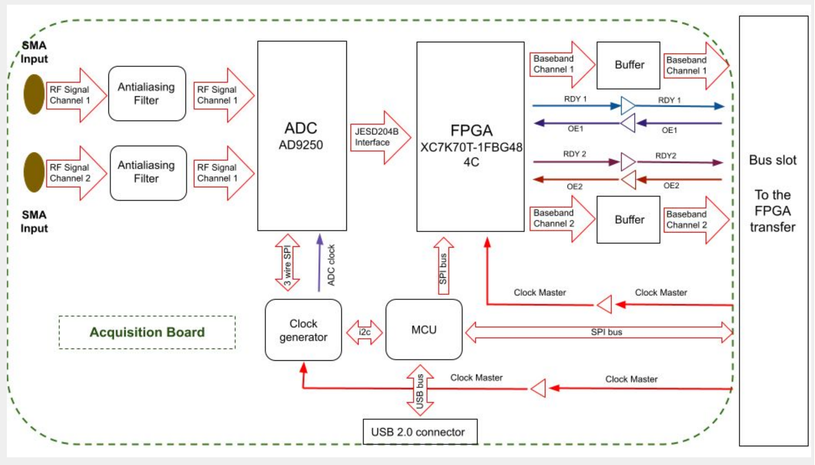


Figure 3. JARS receiver PCB block diagram.

3. FPGA internal architecture

Figure 4 shows how we design the internal logic architecture of the FPGA, we are using all the DSP blocks needed to process the radar data. These blocks will be duplicated for the other channel on the PCB.

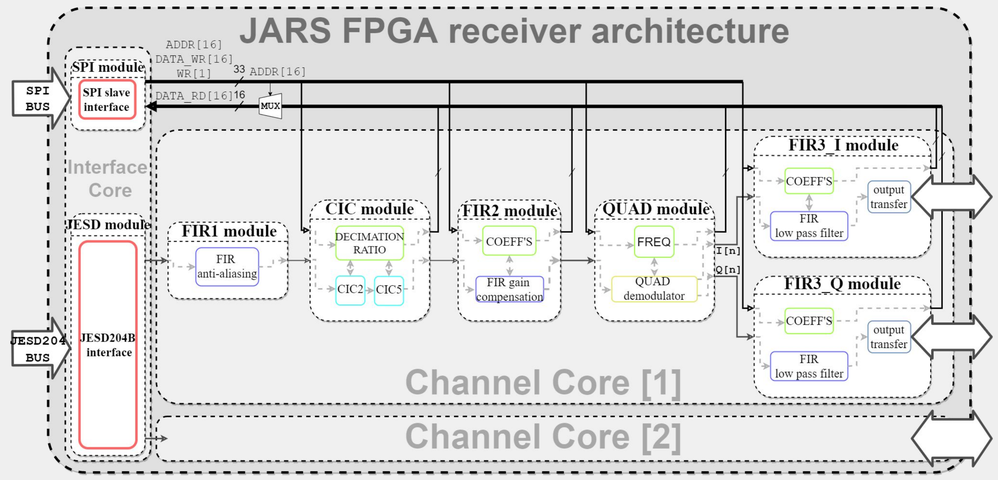


Figure 4. FPGA internal architecture.

4. Conclusions

Our proposal is currently in the design stage, in Figure 5 we present a list of current JARS issues and how they will be fixed with our proposed design.

Issue	Solution
80KHz and harmonics interference.	Control over DSP operations inside the FPGA.
AD6620 bandwidth limitation.	Almost four times the bandwidth of old JARS with the AD9250.
DC level.	More careful analog design.
Voltage magnitude equalization between channels.	More careful and simplified analog design.
60MHz clock interference.	Using PLLs for generating local clocks.
Filter size limitations.	Using the FPGA for making flexible filter designs.
Clock frequency limitation.	Using PLLs to generate clock signals locally.
No antialiasing filter on the input.	Including an analog antialiasing filter.
Fixed DSP hardware implementation.	Control over DSP operations inside the FPGA.
Sticky logic control hardware.	Using the FPGA to manage the control logic.

Figure 5. Comparative table

5. References

[1] Texas Instruments, "ADC14X250 14-Bit 250 MSPS Single Channel ADC With 5 Gb/s JESD204B Output", ADC14X250 datasheet, Dec. 2015 [Revised Apr. 2017].
[2] Analog Devices, "JESD204 Interface Framework", 06 May 2021 https://wiki.analog.com/resources/fpga/peripherals/jesd204
[3] Xilinx, "7 Series FPGAs GTX/GTH Transceivers", 7 Series User Guide, Mar. 2011 [Revised Aug. 2018].
[4] J. Rojas, J. Verástegui and M. Milla, "Design and implementation of a high speed interface system over Gigabit Ethernet based on FPGA for use on radar acquisition systems," 2017 Electronic Congress (E-CON UNI), 2017, pp. 1-4, doi: 10.1109/ECON.2017.8247311.

email: jverastegui@igp.gob.pe